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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/785,094	02/25/2004	Chih An Yang	2019-0235P	8501

2292 7590 02/10/2006

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
ABRAHAM, FETSUM	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 02/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/785,094	YANG, CHIH AN	
	Examiner	Art Unit	
	Fetsum Abraham	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 3-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 3-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Final rejection

Acknowledgement of the terminal disclaimer applied on 12/20/05 is hereby made and the double patenting rejection issued on the final rejection sent on 9/21/05 withdrawn. The terminal disclaimer has overcome the final rejection.

As a preliminary matter, the final rejection given in this action is a result of new search and necessitated by the amended claims in the past from their originally presented form.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al (5,449,948).

As for claims 3,4,8,9, the patent discloses the following:

ABSTRACT:

Integrated circuit devices, chips and methods of making and operating them are disclosed. The devices are specially adapted for high frequency operation e.g. at or above 1 GHz. Inductive noise caused by switching at these frequencies--and which can interfere with switching--is inhibited by using a large bypass capacitor connected between power and ground connections outside the chip, and a small bypass capacitor connected between the same power and ground connections but formed inside the chip. The smaller capacitor cuts noise attributable to the wiring between the larger capacitor and the chip. The chip can have many of the smaller capacitors, even one or more per gate. In the preferred embodiments, the small capacitors from power and ground bonding pads are formed at the front surface of the chip substrate.'

From the Abstract, it is clear there exists an inductive noise eliminating system associated with a chip, the noise eliminating devices being capacitors having power terminals connected to the power supply in the circuit and ground terminals to the ground power of the circuit. Although the abstract teaches that the large capacitor may be formed outside the chip and the small capacitor inside the chip, it, however, provides important information in that two capacitors are used at least in this embodiment. Furthermore, an alternate embodiment is provided such that " The chip can have many of the smaller capacitors, even one or more per gate. In the preferred embodiments, the small capacitors from power and ground bonding pads are formed at the front surface of the chip substrate." thereby asserting that such capacitors can be formed at the surface of the chip. This structural configuration may be apparent from figure 15 where the capacitors were built on the surface of the chip. The following is what the inventor taught to that effect:

A plurality of individual capacitors C1-C6 are provided at the chip surface, separated from wiring line 34 by low-permittivity layer 33 and positioned adjacent but not connected to terminals 94. In this embodiment, the ground capacitor electrodes are the innermost ones, unlike the previous embodiments. Furthermore, although as seen in the figure the lower electrodes 92 appear to be separate, they are in fact joined in common by a connection, which passes round the terminals 94 and does not show because of the section taken. The power electrodes 90, at the surface, are separate. The low-permittivity layer 33 is provided because, as in the first and second embodiments, the capacitors have been formed over a region of substrate including internal circuitry.

In light of those teachings, it is clear that the following issues are most relevant to this application:

a) the fact that there are capacitors (at least two) in the prior art that are used to reduce inductive noise associated with chip circuitry.

b) the fact that the capacitors can be formed on the surface of the chip and having their power terminals connected to the power supply and their ground terminals to the ground power supply of the circuit.

The prior art therefor teaches all subject matter except said " guiding devices" in such a way the claimed invention presents them to be. However, those devices are found to be wiring structures that connect the power and ground terminals of the capacitors to the power supply terminals. Therefore, it would have been obvious to one skilled in the art to safely conclude that the prior art structure also uses wires to maintain the same connections between capacitive terminals and power supply terminals and that regardless of the terminology used for those wirings, the wires serve similar purposes as that in the claimed invention to be classified as power guiding devices based on the applicant' s definition of the wiring structures.

As for claim 5, metal conductors maintain the power interconnections of the prior art circuit.

As for claims 6, 7, **"product by process"** claims are directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685 and In re Thorpe, 227 USPQ 964, 966. Therefore, the way the product was made does not carry any patentable weight as long as the claims are directed to a device. Further, note that the applicant has the burden of proof in such cases, as the above case law makes clear. Also see MPEP 2113.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

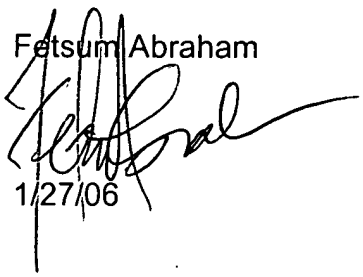
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fetsum Abraham whose telephone number is: 571-272-1911. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915.

Fetsum Abraham



1/27/06